

MOS FIELD EFFECT TRANSISTOR

2SK3365

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK3365 is N-Channel MOS Field Effect Transistor designed for DC/DC converters application of notebook computers.

FEATURES

- Low on-resistance
 $R_{DS(on)1} = 14 \text{ m}\Omega$ (MAX.) ($V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$)
 $R_{DS(on)2} = 21 \text{ m}\Omega$ (MAX.) ($V_{GS} = 4.5 \text{ V}$, $I_D = 15 \text{ A}$)
 $R_{DS(on)3} = 29 \text{ m}\Omega$ (MAX.) ($V_{GS} = 4.0 \text{ V}$, $I_D = 15 \text{ A}$)
- Low C_{iss} : $C_{iss} = 1300 \text{ pF}$ (TYP.)
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3365	TO-251
2SK3365-Z	TO-252

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 30	A
Drain Current (Pulse) ^{Note}	$I_{D(pulse)}$	± 120	A
Total Power Dissipation ($T_C = 25 \text{ }^\circ\text{C}$)	P_T	36	W
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$)	P_T	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

Note $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1 \%$

THERMAL RESISTANCE

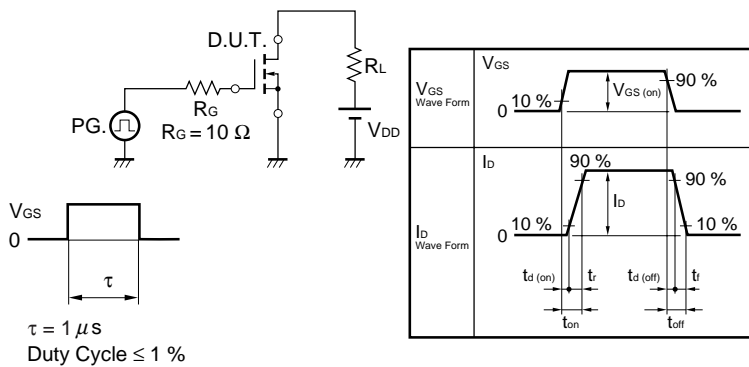
Channel to case	$R_{th(ch-C)}$	3.48	$^\circ\text{C/W}$
Channel to ambient	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

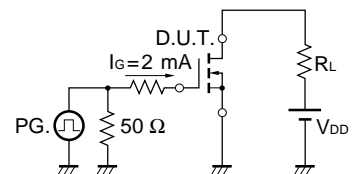
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 15 A		11.5	14	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 15 A		15.2	21	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 15 A		18	29	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 15 A	8.0	16.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		1300		pF
Output Capacitance	C _{oSS}			405		pF
Reverse Transfer Capacitance	C _{rSS}			190		pF
Turn-on Delay Time	t _{d(on)}	I _D = 15 A, V _{GS(on)} = 10 V, V _{DD} = 15 V, R _G = 10 Ω		37		ns
Rise Time	t _r			500		ns
Turn-off Delay Time	t _{d(off)}			75		ns
Fall Time	t _f			95		ns
Total Gate Charge	Q _G	I _D = 30 A, V _{DD} = 24 V, V _{GS} = 10 V		25		nC
Gate to Source Charge	Q _{GS}			4.5		nC
Gate to Drain Charge	Q _{GD}			7.0		nC
Body Diode forward Voltage	V _{F(S-D)}	I _F = 30 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 30 A, V _{GS} = 0 V di/dt = 100 A/μs		35		ns
Reverse Recovery Charge	Q _{rr}			32		nC

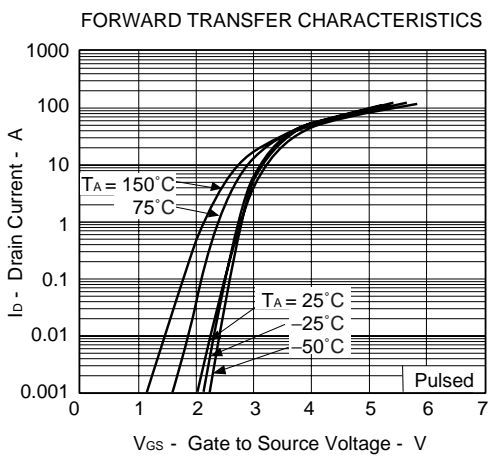
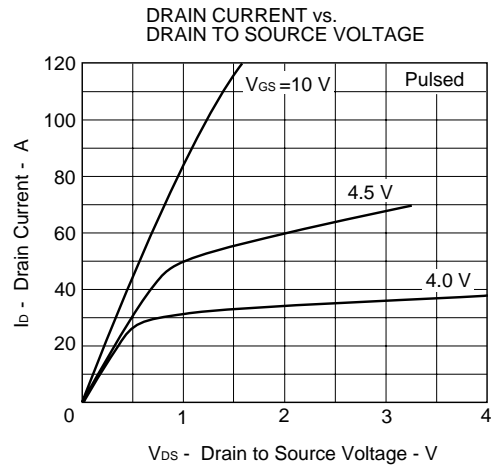
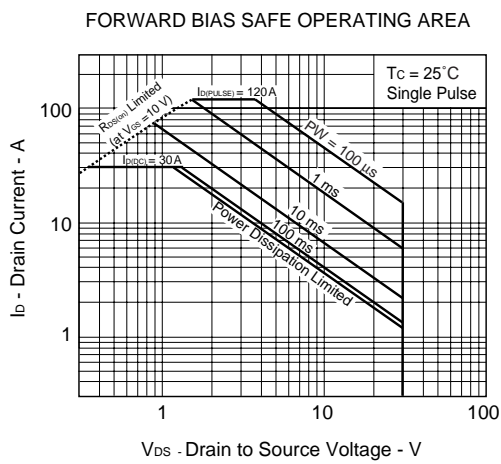
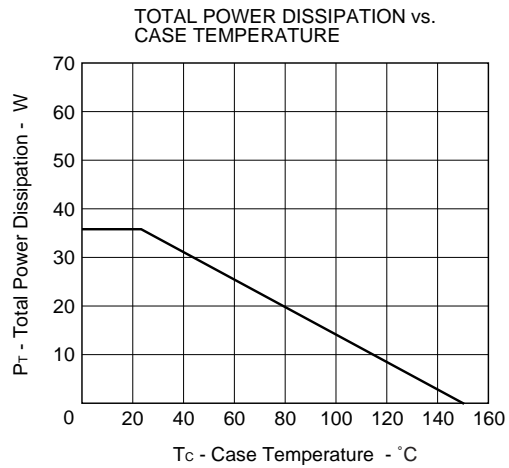
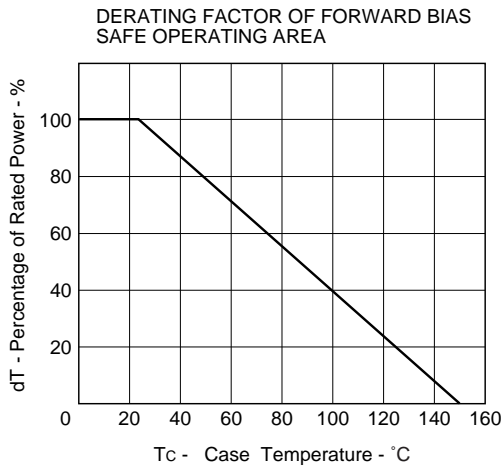
TEST CIRCUIT 1 SWITCHING TIME



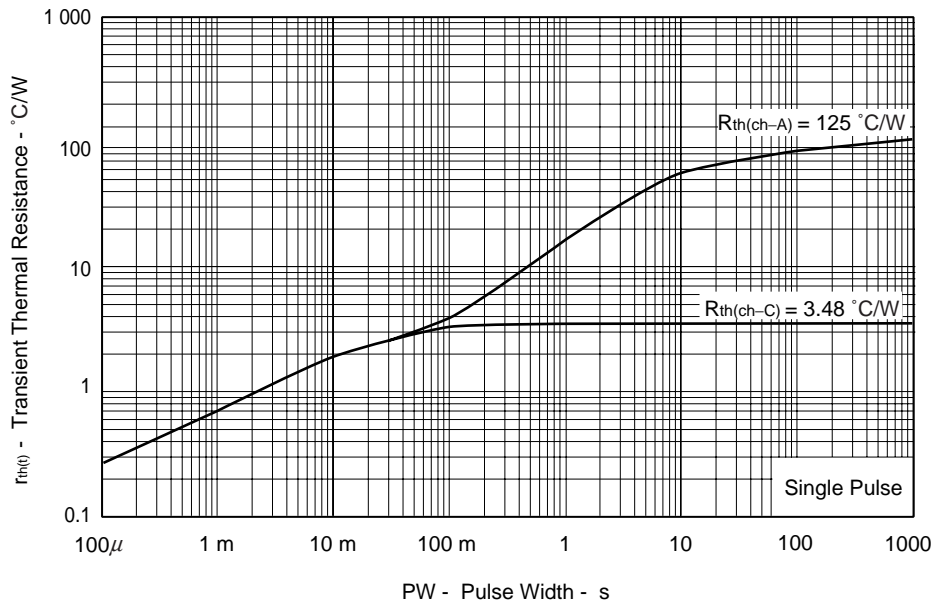
TEST CIRCUIT 2 GATE CHARGE



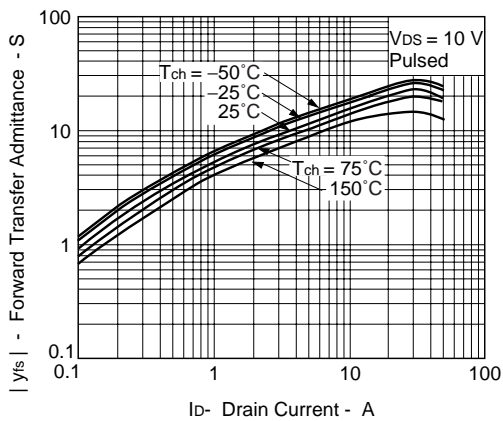
TYPICAL CHARACTERISTICS (T_A = 25 °C)



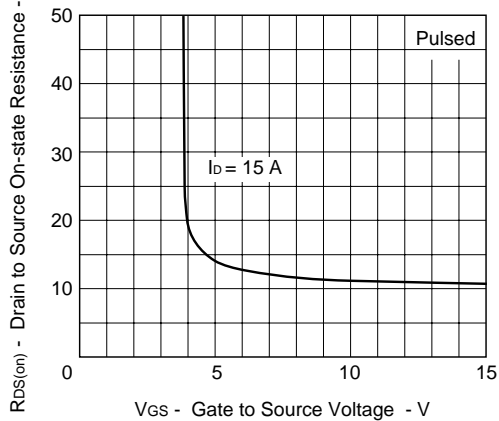
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



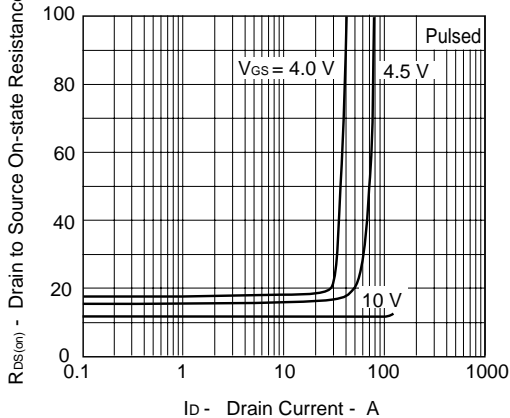
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



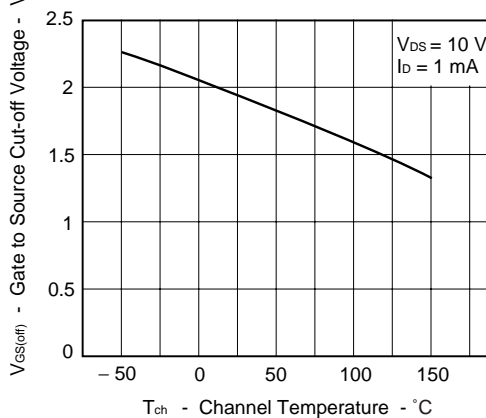
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



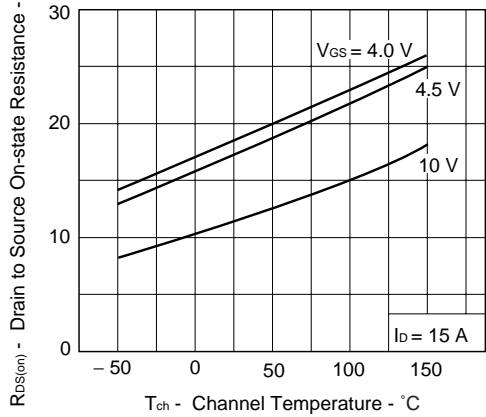
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



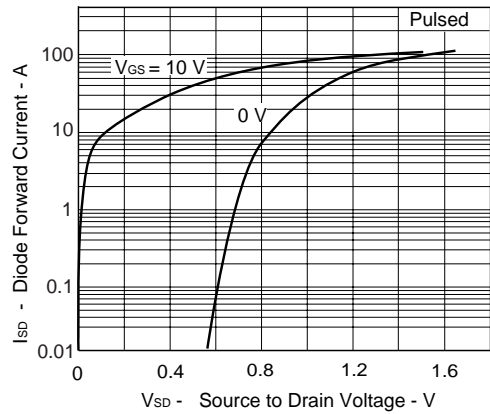
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



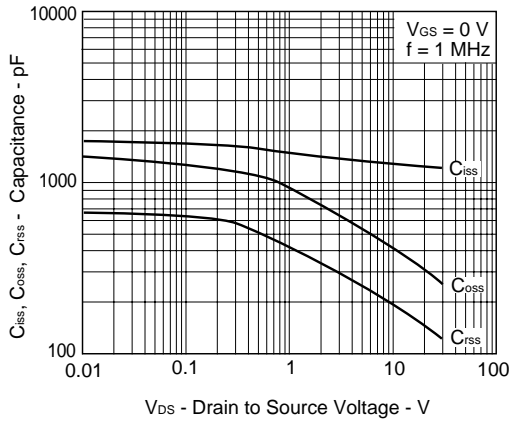
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



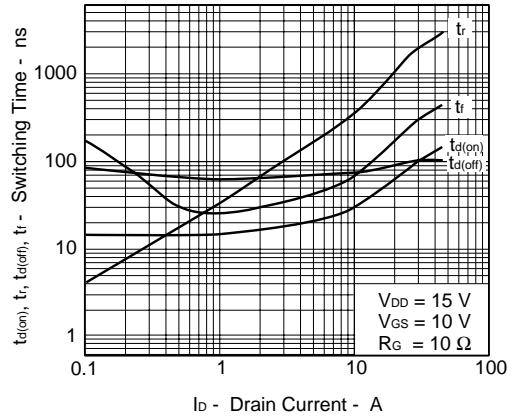
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



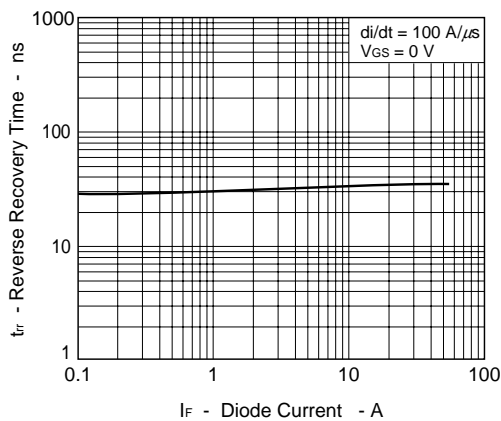
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



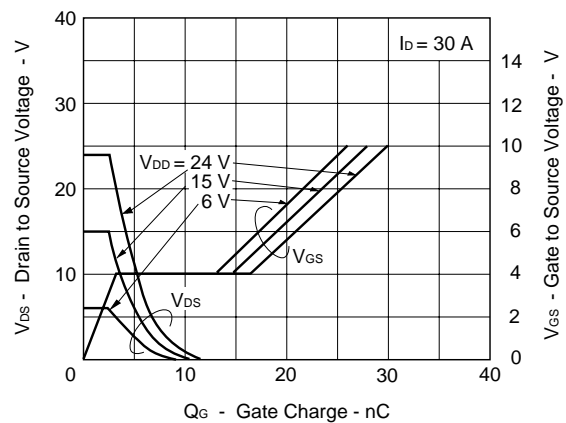
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT

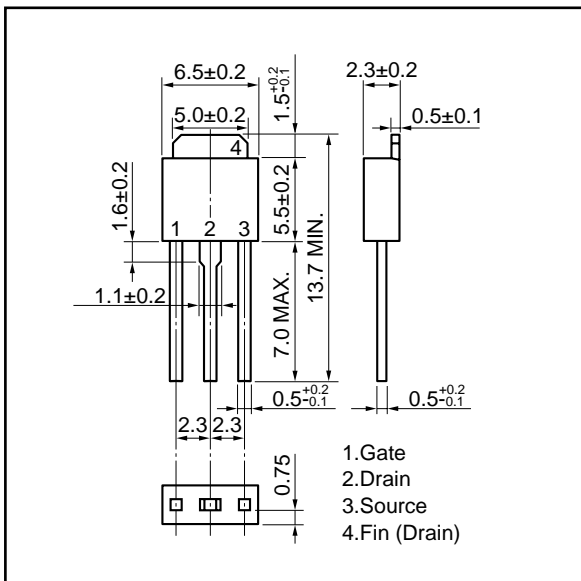


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

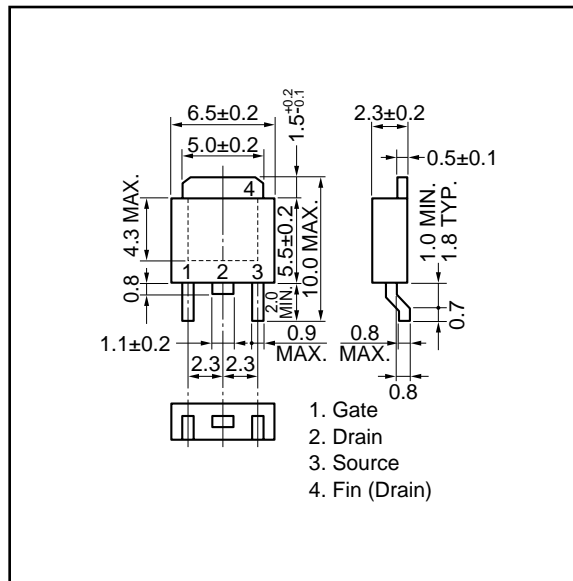


PACKAGE DRAWINGS (Unit : mm)

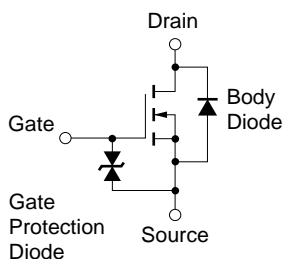
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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